

**Table 7-21** (continued)  
Auxiliary slot signals

Pin	Signal	Description
35	R/W80	Read/write signal for RAM on the card in this slot. This line can drive two LS TTL loads.
36	ø1	65C02 clock phase 1. This line can drive two LS TTL loads.
37	CASEN'	Column-address enable. This signal is disabled (held high) during accesses to memory on the card in this slot. This line can drive two LS TTL loads.
47	H0	Low-order horizontal byte counter. This line can drive two LS TTL loads.
50	AN3	Output of annunciator number 3. This line can drive two LS TTL loads.
52	R/W'	65C02 read/write signal. This line can drive two LS TTL loads.
53	Q3	2 MHz asymmetrical clock. This line can drive two LS TTL loads.
54	SEGB	Second low-order vertical-counter bit. This line can drive two LS TTL loads.
55	FRCTXT'	Normally high; pulling this line low enables 14MHz video output even when GR is active.
56,57	RA9',RA10'	Character-generator control signals from the IOU. This line can drive two LS TTL loads.
58	GR	Graphics-mode enable signal. This line can drive two LS TTL loads.
59	7M	7 MHz timing signal. This line can drive two LS TTL loads.
60	ENTMG'	Normally low; pulling this line high disables the master timing from the PAL device. This line has a 1000 ohm pulldown resistor to ground.